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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/520,190	01/04/2005	Josephus Arnoldus Kahlman	NL 020658	7686

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P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

EXAMINER	
HEYI, HENOK G	

ART UNIT	PAPER NUMBER
2627	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/520,190	KAHLMAN, JOSEPHUS ARNOLDUS	
	Examiner	Art Unit	
	HENOK G. HEYI	2627	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01/04/2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 09/22/2008 have been fully considered but they are not persuasive. Applicant argues that Buchschacher does not teach keeping the clock signal in holding states during a holding period during operation as it was before the holding state. However, as previously argued, Buchschacher teaches a capacitor and buffer setting which inherently is capable of holding clock signals for some period (see col 2 lines 54-60). Therefore, examiner stands by the primary reference and all other secondary references used to repeat the claim rejections.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 24 and 25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 17 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Buchschacher et al 6,052,295 (Buchschacher hereinafter).

Regarding claim 17, Buchschacher teaches an electronic circuit comprising conversion means (see Fig. 1 and col 1 lines65-67) for converting an input voltage (Ui, col2 line 4) into an output voltage (Uo, col 2 line 14), said conversion means comprising at least a first energy storage means (a first capacitor C1, col 2 line 55) and a second energy storage means (output capacitor Cout, col 4 line 6) and switching means (Swl, Sw2, Sw3, Sw4 and Sw5, Fig. 2) for periodically coupling said at least first and second energy storage means (C 1, C2) to one another under the control of clock signal so as to store energy in the at least first and second energy storage means (C1, C2) and for transferring at least a portion of the stored energies between the at least first and second energy storage means (instead of programming the desired clock input signals the invention also makes it possible to automatically generate the desired clock input signal. For this, monitoring means must be coupled between the output OP of the voltage converter and an input of the means, col 2 lines 31-36), and clock signal generating means for generating the clock signals, said clock signal generating means keeping the clock signals in holding states during a holding period during operation, said holding states being equal to the state of the respective clock signal immediately before the holding state (The first charge pump CHGPMP1 further comprises a first capacitor C1 and a first buffer BF1 having an input for receiving the clock input signal d1, col 2 lines 54-60).

Regarding claim 18, Buchschacher teaches the electronic circuit as claimed in claim 17, wherein the switching means and the at least first and second energy storage

means are implemented with the use of at least one charge pump (CHGPMP1 - CHGPMP4, col 2 lines 45-65).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 19 and 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buchschacher in view of Lenssen et al. 6,986,151 B2 (Lenssen hereinafter).

Regarding claim 19, Buchschacher teaches an integrated circuit (IC) that comprises an electronic circuit as defined in claim 17 but fails to teach a medium for storing/reading of user information, comprising an integrated circuit (IC) that comprises an electronic circuit. However, Lenssen teaches an information carrier provided with a storage unit, an integrated circuit and a coupling element (col 1 lines 4-5).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the electronic circuit of Buchschacher to make it usable on storage/reading medium as thought by Lenssen. The modification would have been obvious because of the benefit of storing data and energy as taught by Lenssen (col 1 line 64).

Re claim 26, Lenssen teaches the medium as claimed in claim 19, wherein the medium is an optical disc having a side for storing and reading the user information, wherein the integrated circuit is fastened to said side of the optical disc in a region not reserved for storing and reading of the user information (see 10, Fig. 1).

Regarding claim 27, Lenssen teaches the medium as claimed in claim 19, wherein the medium is an optical disc having a first side for storing and reading of the user information, wherein the integrated circuit is fastened to a second side of the optical disc (see 10, Fig. 3).

Regarding claim 28, Lenssen teaches a recording/playback device comprising means for storing/reading of information onto/from the medium as claimed in claim 19 (apparatus 40, Fig. 7).

Claims 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buchschacher in view of Lenssen and further in view of Dierschke et al. 5,567,976 (Dierschke hereinafter).

Regarding claim 20, Buchschacher teaches providing the input voltage (Ui) from the voltage source and Lenssen teaches an information carrier provided with a storage unit, an integrated circuit and a coupling element but both Buchschacher and Lenssen fail to teach a medium as claimed in claim 19, wherein the integrated circuit (IC) comprises a photosensitive sensor (SNS) for providing the input voltage (Ui) when the sensor (SNS) receives a substantial quantity of light. However, the use of

photosensitive sensors in ICs is well known in the art, and as an example Dierschke teaches integrated circuits including photosensitive sensors.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the electronic circuit of Buchschacher to have a photosensitive sensor thereby to control the input voltage based on the quantity of light. The modification would have been obvious because of the benefit of photosensitive sensors not only for position sensing but also light sensing and voltage controlling.

Regarding claim 21, Lenssen teach the medium as claimed in claim 20, wherein the integrated circuit (IC) furthermore comprises memory means (MM) provided with a supply voltage through utilization of the output voltage (one IC comprising an electrically programmable memory and the other IC a preprogrammed memory, col 3 line 40).

Regarding claim 22, Lenssen teaches the medium as claimed in claim 21, wherein the integrated circuit further comprises a microprocessor, said microprocessor processing the additional information, and said microprocessor being coupled to the memory means for storing the processed additional information (the IC comprises a micro-processor by means of which algorithms can be carried out, and a memory, col 3 lines 25-27) but fails to teach a photosensitive sensor for providing additional information to the microprocessor. However, the use of photosensitive sensors in ICs is well known in the art, and as an example Dierschke teaches integrated circuits including photosensitive sensors.

Regarding claim 23, Lenssen teaches the medium as claimed in claim 21, wherein the integrated circuit further comprises a microprocessor, and in that the microprocessor being coupled to the memory means for processing the additional information after reading of the additional information from the memory means (the IC comprises a micro-processor by means of which algorithms can be carried out, and a memory, col 3 lines 25-27) but fails to teach a photosensitive sensor for providing additional information to the memory means for the storage of the additional information. However, the use of photosensitive sensors in ICs is well known in the art, and as an example Dierschke teaches integrated circuits including photosensitive sensors.

Claims 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buchschacher in view of Lenssen and Dierschke as applied to claim 4 above, and further in view of Miyagi et al. 5955687 (Miyagi hereinafter).

Regarding claim 24, Buchschacher, Lenssen and Dierschke teach the medium as claimed in claim 22, but all three references individually or combined fail to teach that the medium wherein the length of the holding period corresponds by approximation to that of a time period during which the photosensitive sensor does not receive a substantial quantity of light to provide the input voltage. However, Miyagi teaches light sensor which outputs a voltage or a current signal corresponding to the variable quantity of received light (col 15 lines 43-45).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the medium taught by Buchschacher, Lenssen and Dierschke to be able to control the holding period using a photosensitive sensor that regulated voltage based on the amount of light received. The modification would have been obvious for the benefit of outputting voltage corresponding to the amount of light received as taught by Miyagi.

Re claim 25, Lenssen teaches the medium as claimed in claim 24, with a microprocessor and it is fairly obvious for one skilled in the art the microprocessor would be idle during the holding period and Buchschacher teaches that the integrated circuit further comprises a standby circuit for supplying the microprocessor with a supply voltage during the holding period (RT) by activating selected ones from the plurality of the voltage multipliers (col 1 lines 27-30).

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HENOK G. HEYI whose telephone number is (571)270-1816. The examiner can normally be reached on Monday to Friday 8:30 to 5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Joseph Feild can be reached on (571) 272-4090. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Joseph H. Feild/
Supervisory Patent Examiner, Art Unit 2627

/Henok G Heyi/
Examiner, Art Unit 2627